WHAT IS CLAIMED IS:

1. An image processing apparatus comprising:

a first bus which is connected to a coding/decoding unit of image data;

a second bus which is connected to an image memory for storing the image data and used for transferring the image data;

a third bus connected to a CPU for executing a coding process of said image data in accordance with a predetermined program; and

switching control means for arbitrating connecting requests from said CPU and said coding/decoding unit to said image memory and switching the connections of the buses, thereby enabling the image data to be coded by using said first bus during transfer of the image data using said second bus in accordance with a control by said CPU through said third bus.

2. An apparatus according to claim 1, wherein the image data is coded by said coding/decoding unit by using said second bus in parallel with the image data transfer using said second bus.

3. An apparatus according to claim 1, wherein said switching control means further comprises:

memory control means, connected to said second bus, for controlling said image memory; and

bus control means which is connected to said first and third buses and further connected to said memory control means through a fourth bus.

4. An apparatus according to claim 3, further comprising:

image interface means for connecting an image input apparatus or image output apparatus and transmitting and receiving the image data to/from the connected apparatus; and

transfer control means for controlling the image data transfer between said image memory and said apparatus connected to said image interface means through said switching control means.

5. An apparatus according to claim 4, wherein said switching control means further has a cache memory.

6. An apparatus according to claim 4, wherein said transfer control means discriminates an amount of image data stored in said image memory, and when said image data amount reaches an amount by which said image output apparatus can output an image at a predetermined speed irrespective of a difference of processing speeds of said image input apparatus and said image output apparatus, said image data is transferred from said image memory to said image output

apparatus through said switching control means.

7. An apparatus according to claim 3, wherein said switching control means has a crossbar switch.

8. An image processing method comprising:

a first step of receiving a first connecting request to an image memory which is connected to a second bus from image data coding/decoding means which is connected to a first bus and a second connecting request to said image memory from a CPU, connected to a third bus, for executing a coding process of said image data in accordance with a predetermined program; and

a second step of arbitrating said first and second connecting requests and switching the connections of said buses.

9. A method according to claim 8, further comprising:

a third step of performing the image data coding by said coding/decoding means by using said first bus in accordance with a control by said CPU through said third bus in parallel with an image data transfer using said second bus.

10. A method according to claim 9, further comprising:

a transfer step of transferring said image data to/from said image memory by memory control means, connected to said second bus, for controlling said image memory and bus switching means which is connected to said first and third buses and, further, connected to said memory control means through a fourth bus and controlling the data transfer between an image input apparatus and an image output apparatus.

11. A method according to claim 10, wherein said transfer step further comprising the steps of:

discriminating an amount of image data stored in said image memory;

and transferring said image data from said image memory to said image output apparatus when said image data amount reaches an amount by which said image output apparatus can output an image at a predetermined speed irrespective of a difference of processing speeds of said image input apparatus and said image output apparatus.

12. An image processing apparatus having first coding/decoding means and second coding/decoding means, comprising:

at least four buses, that is,

a first bus connected to said first coding/decoding means,

a second bus connected to said second coding/decoding means,

a third bus connected to an image memory for storing image data, and

a fourth bus to which an image input apparatus and an image output apparatus are connected;

a bus bridge for forming data transfer channels between the different buses in response to a request from a bus master on one of at least said four buses, wherein said bus bridge simultaneously forms two or more data transfer channels; and

arbitrating means for arbitrating a plurality of requests from the bus master on one of at least said four buses when said data transfer channel is formed by said bus bridge.

13. An apparatus according to claim 12, wherein a transfer amount of the image data to/from said second coding/decoding means is controlled by said first coding/decoding means.

14. An apparatus according to claim 13, wherein said first coding/decoding means executes a coding/decoding process of the image data by a CPU for managing a whole control of said image processing apparatus.